Takahata. The Applicant respectfully traverses the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

There is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Yamazaki and Takahata or to combine reference teachings to achieve the claimed invention. MPEP § 2142 states that the examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. It is respectfully submitted that the Official Action has failed to carry this burden. While the Official Action relies on various teachings of the cited prior art to disclose aspects of the claimed invention and asserts that these aspects could be used together, it is submitted that the Official Action does not adequately set forth why one of skill in the art would combine the references to achieve the features of the present invention.

The test for obviousness is not whether the references "could have been" combined or modified as asserted in the Official Action, but rather whether the references should have been. As noted in MPEP § 2143.01, "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990) (emphasis in original). Thus, it is respectfully submitted that the standard set forth in the Official Action is improper to support a finding of *prima facie* obviousness.

The claims of the present application are supported in the present specification, for example, by Figures 10 and 11 and the description in the specification beginning at page 24. For example, the present invention is directed to a semiconductor device comprising: a substrate (e.g. 101) having an insulating surface; at least first and second semiconductor islands (e.g. 104) formed over said substrate wherein each of the semiconductor islands has a channel region and a pair of impurity regions; an insulating film (e.g. 105) formed over said substrate, said insulating film including at least first and second gate insulating films formed over said first and second semiconductor islands, respectively; at least first and second gate electrodes (e.g. 106) formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween; a wiring (e.g. 109) formed on said insulating film for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode wherein said wiring is connected to said one of the impurity regions through a hole opened in said insulating film; a data line (e.g. 110) formed on said insulating film connected to the other one of the impurity regions of the first semiconductor island; a first interlayer insulating film (e.g. 111) formed over the first and second semiconductor islands, the first and second gate electrodes, the wiring and the data line; a voltage supply line (e.g. 112) formed on said first interlayer insulating film connected to one of the pair of impurity regions of the second semiconductor island; a second interlayer insulating film (e.g. 114) formed over said first interlayer insulating

film and said voltage supply line; a pixel electrode (e.g. 115) formed over said second interlayer insulating film connected to the other one of the pair of the impurity regions of the second semiconductor island.

The Official Action appears to compare Figure 8 of Yamazaki with the present claims. Specifically, the Official Action alleges that the source electrode 36b' of Yamazaki corresponds with the wiring (e.g. 109) of the present claims and that the source electrode 36b corresponds with the voltage supply line (e.g. 112) of the present claims (pages 2-4, Paper No. 20060606). The Official Action correctly admits that Yamazaki "lacks anticipation of a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode" (pages 3 and 4; Id.). That is, the Official Action appears to concede that source electrode 36b', which is relied upon to allegedly correspond with the wiring of the present claims, is not for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode. The Official Action relies on Figure 2 of Takahata to allegedly teach "a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode" (page 3 and 5, Id.). The Official Action asserts that "it would have been obvious ... to modify Yamazaki's device by incorporating Takahata teachings sine that would enhance speed as taught by Takahata" (Id.). The Applicant respectfully disagrees and traverses the above assertions in the Official Action.

In order to render obvious the present invention, the Official Action would need to present a suggestion or motivation to modify Figure 8 of Yamazaki such that the source electrode 36b' electrically connects one of the impurity regions 34b' of the first semiconductor island (left side of Figure 8(F)) with the second gate terminal 40. Takahata does not teach or suggest such a modification to Yamazaki, because such a modification would change the intended function of Yamazaki. Takahata does not teach or suggest that the configuration, such as that shown in Figure 8 of Yamazaki, could or should be modified to match the configuration shown in Figure 2 of Takahata.

Specifically, if Yamazaki were modified so that the source electrode 36b' is connected to the gate terminal 40 of the second transistor, Yamazaki would not perform its intended function after modification. The intended function of Yamazaki would, at least, be modified, if not destroyed. The embodiment of Figure 8 of Yamazaki is related to a circuit configuration shown in Figure 3 of Yamazaki. The Applicant respectfully submits that there is insufficient motivation that would suggest to one of ordinary skill in the art at the time of the present invention to modify the circuit of Figure 3 of Yamazaki so that one of the impurity regions of the first transistor is connected to a gate of a second transistor.

Also, in the "Response to Arguments" section, the Official Action asserts that "Yamazaki does not teach away from such modification" (page 6, Paper No. 20060606). This statement is insufficient to support a *prima facie* case of obviousness. It is not sufficient to assert that a reference could have been modified. Rather, a *prima facie* case of obviousness requires that the Examiner show the reference should have been modified in the manner asserted in the Official Action. Yamazaki and Takahata do not contain sufficient motivation to teach or suggest why one of ordinary skill in the art at the time of the present invention would have been motivated to electrically connect one of the impurity regions 34b' of the first semiconductor island (left side of Figure 8(F) of Yamazaki) with the second gate terminal 40 using the source electrode 36b', particularly when such modification changes the intended function of Yamazaki.

Therefore, the Applicant respectfully submits that the Official Action has not provided a proper or sufficient suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Yamazaki and Takahata or to combine reference teachings to achieve the claimed invention.

In the present application, it is respectfully submitted that the prior art of record, either alone or in combination, does not expressly or impliedly suggest the claimed invention and the Official Action has not presented a convincing line of reasoning as to

why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

Also, Yamazaki and Takahata do not teach or suggest all the features of the present claims. In addition to those deficiencies in Yamazaki noted above, there are additional differences between Yamazaki and the present claims, which are not addressed in the Official Action and are not cured by the disclosure of Takahata. For example, the Official Action relies on source electrode 36b' to correspond with the claimed wiring and on silicon oxide film 35 to correspond with the claimed insulating film (pages 2 and 4, Paper No. 20060606); however, the source electrode 36b' is not formed on the silicon oxide film 35. The Official Action relies on drain electrode 36a' to correspond with the claimed data line (Id.); however, the drain electrode 36a' is not formed on the silicon oxide film 35. The Official Action relies on source electrode 36b to correspond with the claimed voltage supply line and on interlayer insulating film 37 (presumably the first occurrence in Figure 8(E)) to correspond with the claimed first interlayer insulating film (Id.); however, source electrode 36b is not formed on the interlayer insulating film 37. The Official Action relies on lead electrode 37 (presumably the second occurrence in Figure 8(F)) to correspond with the claimed pixel electrode (Id.); however, the lead electrode 37 appears to be connected to the same impurity region of the second semiconductor island as the source electrode (voltage supply line) 36b. Yamazaki and Takahata, either alone or in combination, do not teach or suggest modifying Yamazaki so that the source electrode 36b' is formed on the silicon oxide film 35; so that the drain electrode 36a' is formed on the silicon oxide film 35; so that the source electrode 36b is formed on the interlayer insulating film 37; and so that the source electrode (voltage supply line) 36b is connected to one impurity region of the second semiconductor island while the lead electrode 37 is connected to the other impurity region of the second semiconductor island.

For the reasons stated above, the Official Action has not formed a proper *prima facie* case of obviousness. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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